

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kevin W. Glass et al.

Title: BIASED DARLINGTON TRANSISTOR PAIR, METHOD, AND SYSTEM

Docket No.: 80107.099US1

Serial No.: 10/727262

Filed: December 3, 2003

Due Date: N/A

Examiner: Unknown

Group Art Unit: 2817

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

☒ A return postcard.

☒ An Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 4 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 50-2359.

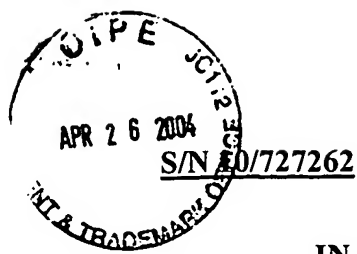
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By: Dana B. LeMoine
Atty: Dana LeMoine
Reg. No. 40,062

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20th day of April, 2004.

Andrew J. Kov
Name

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PATENT

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Serial No.:	10/727262	Group Art Unit:	2817
Filed:	December 03, 2003	Docket:	80107.099US1
Title:	BIASED DARLINGTON TRANSISTOR PAIR, METHOD, AND SYSTEM		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 50-2359 in order to have this Information Disclosure Statement considered.

Information Disclosure Statement

Serial No. 10/727262

Date Filed: December 03, 2003

Title: BIASED DARLINGTON TRANSISTOR PAIR, METHOD, AND SYSTEM

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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

KEVIN W. GLASS ET AL.

By their Representatives,

LeMoine Patent Services, PLLC
c/o PortfolioIP
P.O. Box 52050
Minneapolis, MN 55402
952-473-8800

Date 4-19-04

By Dana B. LeMoine
Dana LeMoine
Reg. No. 40,062

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Andrew J. Kaul
Name

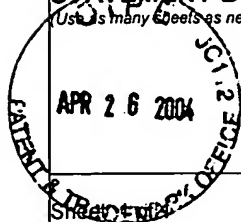
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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	10/727262
Filing Date	December 3, 2003
First Named Inventor	Glass, Kevin
Group Art Unit	2817
Examiner Name	Unknown

Attorney Docket No: 80107.099US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁴
		BOLES, TIMOTHY, "A Fully Monolithic HMIC Low Noise Amplifier", <u>Radio Frequency Integrated Circuits (RFIC) Symposium</u> , (June 1997), pp. 109-112	
		HODGES, DAVID A., "Darlington's Contributions to Transistor Circuit Design", <u>IEEE Transactions on Circuits and Systems - I: Fundamental Theory and Applications</u> , Volume 46, No. 1, (January 1999), pp. 102-104	
		TRAJKOVIC, LJILJANA, et al., "Replacing a Transistor with a Compound Transistor", <u>IEEE Transactions on Circuits and Systems</u> , Volume 35, No. 9, (September 1988), pp. 1139-1146	
		UMEDA, A Y., et al., "A Monolithic GaAs HBT Upconverter", <u>IEEE Microwave and Millimeter-Wave Monolithic Circuits and Symposium</u> , (May 1990), pp. 77-80	

EXAMINER**DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached